



FIG. 1
PRIOR ART TIMING RECOVERY IN A DIGITAL RECEIVER.

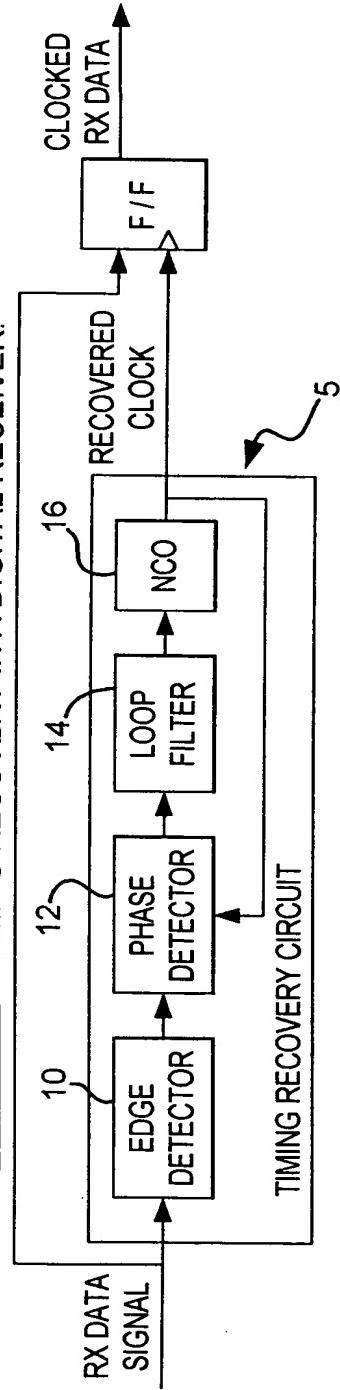


FIG. 2
PRIOR ART
TIMING RECOVERY
WAVEFORMS.

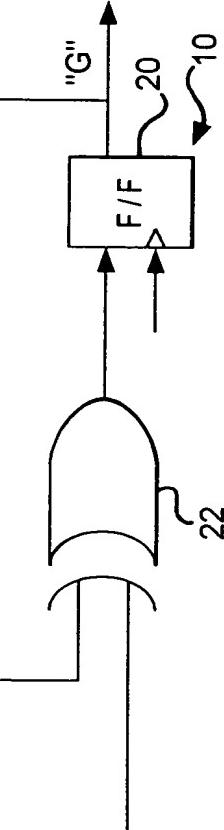
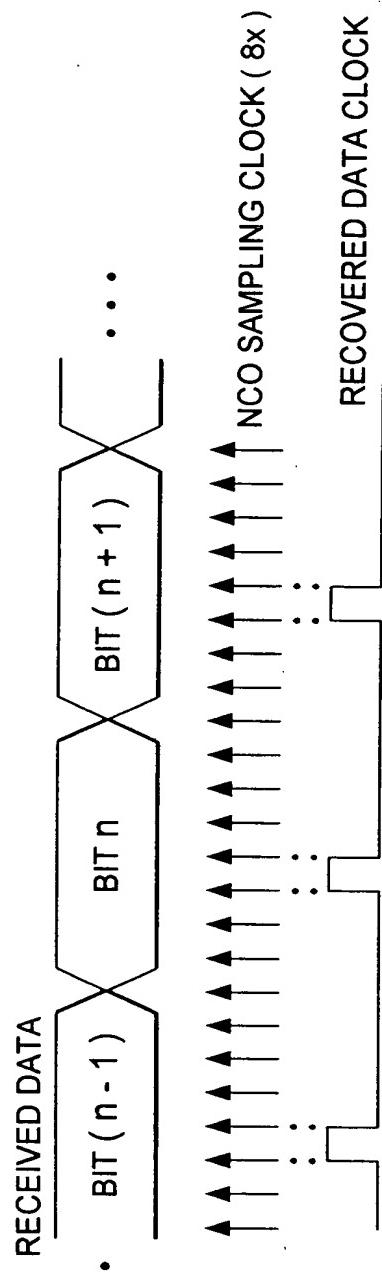


FIG. 3
PRIOR ART
EDGE DETECTOR.

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FIG. 4 NONLINEAR PHASE COUNTER.

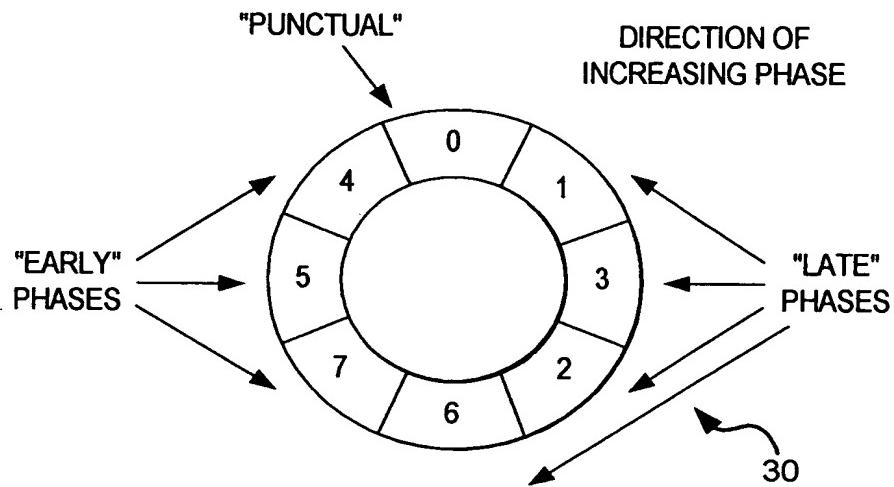
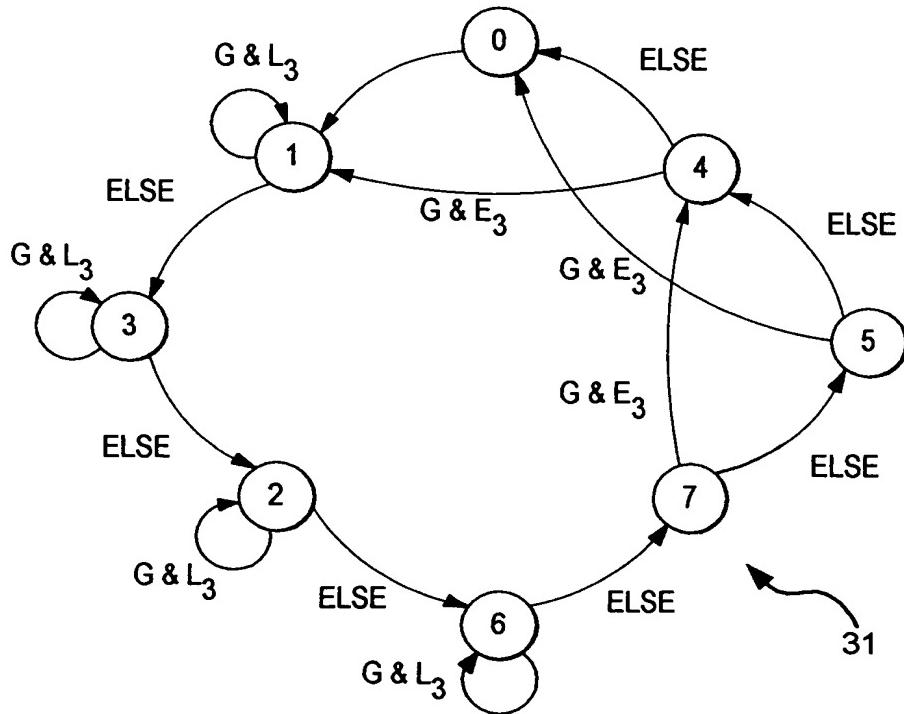


FIG. 5 STATE MACHINE "C", THE PHASE COUNTER.



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FIG. 6 STATE MACHINE "F", THE LOOP COUNTER.

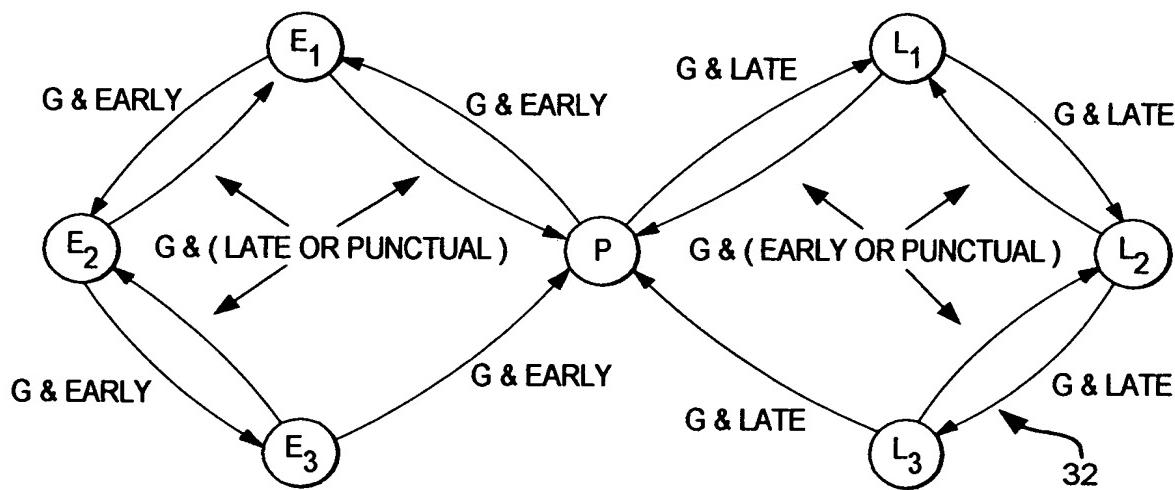


FIG. 7 LOGIC CIRCUIT IMPLEMENTATION OF SIMPLIFIED TIMING RECOVERY CIRCUIT.

